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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,999	02/01/2006	Masaharu Udagawa	39576	9629

52054 7590 05/14/2007

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EXAMINER	
HU, RUI MENG	

ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,999	UDAGAWA ET AL.	
	Examiner	Art Unit	
	RuiMeng Hu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,14 and 16-24* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/1/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement submitted on 2/1/2006 been considered by the Examiner and made of record in the application file.

Drawings

3. **Figures 13-16** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. **Claim 13** is objected to because of the following informalities:

1). Replace "de lay" with --delay--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claims 13-14, 16-22 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Persson (US Patent 7072420)** in view of **McCune et al. (US Patent 6366177).**

Consider **claim 13**, Persson clearly discloses a transmitting apparatus using polar modulation (column 2 lines 1-3), the apparatus comprising: a polar signal producer (figure 1, RF circuit 1, column 3 lines 15-21), producing signals corresponding to an amplitude and a phase of a transmitting modulated signal from an input signal (figure 1, r_4 and ϕ_4).

Persson discloses (column 3 lines 15-21) the operation of the RF circuitry is well known in the art, in the same field of endeavor, McCune et al. clearly disclose the details of polar modulation. An amplitude signal producer (McCune et al. figure 11, magnitude controller 1127 controlling power amplifier for amplitude modulation), producing an amplitude signal from a signal corresponding to the amplitude; a phase-modulated signal producer (McCune et al. figure 11, phase modulation signal generator 1129), producing a phase-modulated signal from a signal corresponding to the phase; an amplitude-modulation amplifier (McCune et al. figure 11, power amplifier 1107), amplitude-modulating the phase-modulated signal (polar modulation) by the amplitude signal and the phase-modulated signal to produce a transmitting modulated signal (McCune et al. figure 11, polar modulated signal output from power amplifier 1107).

Persson further discloses an amplitude/phase detector (figure 1, column 3 lines 48-53, 59-64, delay controllers 9 operate to minimize the magnitude of the difference between r_4 and r_3, and the difference between ϕ_4 and ϕ_3; thus delay controllers 9

have magnitude detection function and indirectly detecting the magnitude of r_1 and ϕ_1), detecting an amplitude signal (r_1) and a phase signal (ϕ_1) from an input signal to the amplitude-modulation amplifier (figure 1, polar signal producer circuit 1) and an input signal to the phase-modulated signal producer (figure 1, polar signal producer circuit 1); a delay difference computer (figure 1, delay calculator 12), computing a delay difference between an amplitude signal and a phase signal based on the signal corresponding to the amplitude and the signal corresponding to the phase (r_4 and ϕ_4), which are produced by the polar signal producer (figure 1, polar signal producer 1), and the amplitude signal and the phase signal (figure 1, r_1 and ϕ_1), which are detected by the amplitude/phase detector (delay controllers 9); and a timing adjustor (figure 1, adjusters 14 and 16), adjusting timings of the amplitude signal and the phase signal based on the delay difference computed by the delay difference computer.

Consider **claim 14 as applied to claim 13**, Persson as modified by McCune et al. clearly discloses wherein the delay difference computer (figure 1, delay calculator 12, adders 10) computes a correlation function (adder 10_2) between the signal corresponding to the amplitude (r_4, output of circuit 3) produced by the polar signal producer (figure 1, polar signal producer circuit 1) and the amplitude signal detected by the amplitude/phase detector (figure 1, Delay controllers 9) and a correlation function (adder 10_1) between the signal corresponding to the phase produced by the polar signal producer and the phase signal detected by the amplitude/phase detector, and computes the quantity of delay of the amplitude signal (output of adder 10_2) and the quantity of delay of the phase signal (output of adder 10_1) from maximum values of the

respective correlation functions related to these amplitude and phase and computes a delay difference (figure 1, delay calculations of circuit 12) from a difference between the quantity of delay of the amplitude signal and the quantity of delay of the phase signal.

Consider **claim 16 as applied to in claim 13**, Persson as modified by McCune et al. clearly discloses wherein the timing adjustor (timing adjusters 14 and 16 are delay units that delaying the input signals based on the control signals outputted from delay controller circuit 12) has a delay unit delaying at least one of the amplitude signal and the phase signal and a delay controller controlling the quantity of delay of the delay unit.

Consider **claim 17 as applied to in claim 13**, Persson as modified by McCune et al. clearly discloses wherein the timing adjustor has a rough adjustor (delay controllers 9) roughly adjusting the quantity of delay of the amplitude signal and the quantity of delay of the phase signal and a fine adjustor (adjusters 14 and 16) finely adjusting the quantity of delay.

Consider **claim 18 as applied to claim 13**, Persson as modified by McCune et al. clearly discloses wherein the timing adjustor is constructed of a digital circuit (figure 5, adjusters 22 and 24 capable of processing I and Q digital signals) and varies a clock frequency of this digital circuit to adjust the quantity of delay of the amplitude signal and the quantity of delay of the phase signal (adjusters 22 and 24 delaying the signals based on control signals outputted from circuit 12, and the teaching of varying a clock frequency to adjust the quantity of delay is well known in the art, a person skilled in the art would recognize these teachings could be utilized in the adjusters 22 and 24 of Persson as modified by McCune et al.).

Consider **claim 19 as applied to claim 16**, Persson as modified by McCune et al. clearly discloses wherein the timing adjustor has a plurality of inverters connected in cascade as the delay unit and a selector for switching outputs of the inverters (these teachings are well known in the art, a person skilled in the art would recognize these teachings could be utilized in the adjusters 22 and 24 of Persson as modified by McCune et al.).

Consider **claim 20 as applied to claim 16**, Persson as modified by McCune et al. clearly discloses wherein the timing adjustor has a digital filter capable of varying a delay time according to a control signal as the delay unit (these teachings are well known in the art, a person skilled in the art would recognize these teachings could be utilized in the adjusters 22 and 24 of Persson as modified by McCune et al.).

Consider **claim 21 as applied to claim 13**, Persson as modified by McCune et al. clearly discloses wherein the amplitude modulation amplifier is configured to have a power amplifier (McCune et al. figure 11, power amplifier 1107).

Consider **claim 22 as applied to claim 13**, Persson as modified by McCune et al. clearly discloses wherein the amplitude modulation amplifier is configured to have a variable gain amplifier (McCune et al. figure 11, variable power amplifier 1107).

Consider **claim 24**, Persson clearly discloses a method of synchronizing an amplitude signal and a phase signal in a transmitting apparatus using polar modulation, (figure 1) the method comprising the steps of: producing signals (figure 1, r_4 and ϕ_4) corresponding to an amplitude and a phase of a transmitting modulated signal from an input signal; producing an amplitude signal (figure 1, r_2) from a signal corresponding to

the amplitude; producing a phase-modulated signal (McCune et al. disclose the detail of polar modulation, figure 11, phase modulation (PM) signal generator 1129 for producing PM signal) from a signal corresponding to the phase; multiplying (figure 1, circuit 1 modulating polar signal by modulating r_2 on top of ϕ_2, thus considered as multiplying) the amplitude signal by the phase-modulated signal to amplitude modulate the phase-modulated signal to produce a transmitting modulated signal; detecting (figure 1, column 3 lines 48-53, 59-64, delay controllers 9 operate to minimize the magnitude of the difference between r_4 and r_3, and the difference between ϕ_4 and ϕ_3; thus delay controllers 9 have magnitude detection function and indirectly detecting the magnitude of r_1 and ϕ_1) an amplitude signal and a phase signal from an amplitude signal (r_1) before the amplitude signal being multiplied by the phase-modulated signal and a signal corresponding to a phase (ϕ_1) before the phase-modulated signal being produced; computing a delay difference (figure 1, circuit 12) between an amplitude signal and a phase signal based on the signal corresponding to the amplitude and the signal corresponding to the phase (r_4 and ϕ_4), which are produced from the input signal, and the amplitude signal and the phase signal, which are detected (r_1 and ϕ_1); and adjusting timings (figure 1, adjusters 14 and 16) of the amplitude signal and the phase signal based on the computed delay difference to synchronize the amplitude signal and the phase signal.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Persson (US Patent 7072420)** as modified by **McCune et al. (US Patent 6366177)** in view of **Bellaouar et al. (US Pub. 2003/0118143).**

Consider **claim 23 as applied to claim 13**, Persson as modified by McCune et al. fails to disclose wherein the amplitude modulation amplifier is configured to have a mixer circuit.

In the same field of endeavor, Bellaouar et al. clearly disclose using a mixer circuit for amplitude modulation (figure 4, mixer 43).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Bellaouar et al. into the art of Persson as modified by McCune et al. as to include a mixer circuit for amplitude modulation as an alternative.

Allowable Subject Matter

10. **Claim 15** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Consider **claim 15 as applied to claim 13**, Persson in view of McCune et al. discloses wherein the amplitude/phase detector (figure 1, delay controllers 9 capable of processing I and Q digital signals) is constructed of a digital circuit.

However Persson as modified by McCune fails to disclose the amplitude/phase detector has a selector selecting either the amplitude signal or the phase signal and an analog-digital converter converting the selected amplitude signal or phase signal provided at an input section of the amplitude signal and the phase signal.

Persson as modified by McCune et al. discloses delay controllers 9 operate to minimize the magnitude of the difference between r_4 and r_3, and the difference between ϕ_4 and ϕ_3. These teachings clearly differ from the claimed invention; therefore, claim 15 of the present application is considered novel and non-obvious over the prior art and, consequently, is allowed.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to:**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RuiMeng Hu whose telephone number is 571-270-1105. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RuiMeng Hu
R.H./rh
May 8, 2007

EDAN ORGAD
PRIMARY PATENT EXAMINER
Edan Orgad 5/8/07